



IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs



Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review

Quick Links

» See

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Table of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced

MEMBER SERVICES

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

ENTERPRISE SERVICES

- Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **39** of **1069805** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

(tanaka<in>au) <and> (watermark* or embed* or steg*)

Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 A remote control system for FPGA-embedded modules in radiation environments

Hasuko, K.; Fukunaga, C.; Ichimiya, R.; Ikeno, M.; Ishida, Y.; Kano, H.; Kurose, H.; Mizouchi, K.; Nakamura, Y.; Sakamoto, H.; Sasaki, O.; Tanaka, K.; Nuclear Science, IEEE Transactions on, Volume: 49, Issue: 2, April 2002
Pages:501 - 506

[\[Abstract\]](#) [\[PDF Full-Text \(271 KB\)\]](#) **IEEE JNL**

2 A 1.8-V embedded 18-Mb DRAM macro with a 9-ns RAS access time memory-cell area efficiency of 33%

Yokoyama, Y.; Itoh, N.; Hasegawa, M.; Katayama, M.; Akasaki, H.; Kaneda, T.; Ueda, T.; Tanaka, Y.; Yamasaki, E.; Todokoro, M.; Toriyama, K.; Miki, H.; Yamada, M.; Takashima, K.; Kobayashi, T.; Miyaoka, S.; Tamba, N.; Solid-State Circuits, IEEE Journal of, Volume: 36, Issue: 3, March 2001
Pages:503 - 509

[\[Abstract\]](#) [\[PDF Full-Text \(192 KB\)\]](#) **IEEE JNL**

3 New noise rejection techniques on pulse-by-pulse basis for on-line partial discharge measurement of turbine generators

Itoh, K.; Kaneda, Y.; Kitamura, S.; Kimura, K.; Nishimura, A.; Tanaka, T.; Tsuchiya, H.; Okada, I.; Energy Conversion, IEEE Transactions on, Volume: 11, Issue: 3, Sept. 1991
Pages:585 - 594

[\[Abstract\]](#) [\[PDF Full-Text \(756 KB\)\]](#) **IEEE JNL**

4 Multichannel fiber ferrule for a stable laser-diode array module

Nakagawa, G.; Miura, K.; Tanaka, K.; Yano, M.;

Photonics Technology Letters, IEEE , Volume: 7 , Issue: 4 , April 1995
Pages:409 - 411

[\[Abstract\]](#) [\[PDF Full-Text \(308 KB\)\]](#) [IEEE JNL](#)

5 DRAM macros for ASIC chips

Sunaga, T.; Miyatake, H.; Kitamura, K.; Kasuya, K.; Saitoh, T.; Tanaka, M.; Tanigaki, N.; Mori, Y.; Yamasaki, N.;
Solid-State Circuits, IEEE Journal of , Volume: 30 , Issue: 9 , Sept. 1995
Pages:1006 - 1014

[\[Abstract\]](#) [\[PDF Full-Text \(832 KB\)\]](#) [IEEE JNL](#)

6 A 34-ns 16-Mb DRAM with controllable voltage down-converter

Hidaka, H.; Arimoto, K.; Hirayama, K.; Hayashikoshi, M.; Asakura, M.; Tsukui, M.; Oishi, T.; Kawai, S.; Suma, K.; Konishi, Y.; Tanaka, K.; Wakamiya, W.; C. Y.; Fujishima, K.;
Solid-State Circuits, IEEE Journal of , Volume: 27 , Issue: 7 , Jul 1992
Pages:1020 - 1027

[\[Abstract\]](#) [\[PDF Full-Text \(1050 KB\)\]](#) [IEEE JNL](#)

7 Computation accuracies of boundary element method and finite element method in transient eddy current analysis

Tsuboi, H.; Tanaka, M.; Misaki, T.; Naito, T.;
Magnetics, IEEE Transactions on , Volume: 24 , Issue: 6 , Nov 1988
Pages:3174 - 3176

[\[Abstract\]](#) [\[PDF Full-Text \(164 KB\)\]](#) [IEEE JNL](#)

8 PLC-type hybrid external cavity laser integrated with front-monitor photodiode on Si platform

Tanaka, T.; Hibino, Y.; Hashimoto, T.; Kasahara, R.; Inoue, Y.; Himeno, A.; Ito, M.; Abe, M.; Oohashi, H.; Tohmori, Y.;
Electronics Letters , Volume: 37 , Issue: 2 , 18 Jan 2001
Pages:95 - 96

[\[Abstract\]](#) [\[PDF Full-Text \(212 KB\)\]](#) [IEEE JNL](#)

9 Improved embedded zerotree wavelet coder

Kang, E.-S.; Tanaka, T.; Ko, S.-J.;
Electronics Letters , Volume: 35 , Issue: 9 , 29 April 1999
Pages:705 - 706

[\[Abstract\]](#) [\[PDF Full-Text \(236 KB\)\]](#) [IEEE JNL](#)

10 A 16 MB cache DRAM LSI with internal 35.8 GB/s memory bandwidth for simultaneous read and write operation

Nakayama, M.; Sakakibara, H.; Kusunoki, M.; Kurita, K.; Yokoyama, Y.; Miyamoto, S.; Koike, J.; Tamba, N.; Kobayashi, T.; Kume, M.; Sawamoto, H.; Kawata, A.; Tanaka, H.; Takada, Y.; Yamamoto, M.; Yagyu, M.; Tsuchiya, Y.; Yoshida, H.; Kitamura, N.; Yamaguchi, K.;
Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000

IEEE International , 7-9 Feb. 2000
Pages:398 - 399, 472-3

[\[Abstract\]](#) [\[PDF Full-Text \(363 KB\)\]](#) [IEEE CNF](#)

11 A novel bit-line process using poly-Si masked dual-damascene (PM for 0.13 µm DRAMs and beyond

Miyashita, T.; Nitta, H.; Nomura, H.; Nakajima, K.; Sakata, A.; Mizutani, T.; Minakata, H.; Tanaka, M.; Tomita, H.; Kurahashi, T.; Watanabe, Y.; Kubota, Hatada, A.; Hosaka, K.; Hashimoto, K.; Kohyama, Y.;
Electron Devices Meeting, 2000. IEDM Technical Digest. International , 10-13 2000
Pages:361 - 364

[\[Abstract\]](#) [\[PDF Full-Text \(384 KB\)\]](#) [IEEE CNF](#)

12 A fabrication method for high performance embedded DRAM of 0.1 generation and beyond

Yoshida, T.; Takato, H.; Sakurai, T.; Kokubun, K.; Hiyama, K.; Nomachi, A.; Takasu, Y.; Kishida, M.; Ohtsuka, H.; Naruse, H.; Morimasa, Y.; Yanagiya, N. Hashimoto, T.; Noguchi, T.; Miyamae, T.; Iwabuchi, N.; Tanaka, M.; Kumaga Ishiuchi, H.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Pages:61 - 64

[\[Abstract\]](#) [\[PDF Full-Text \(268 KB\)\]](#) [IEEE CNF](#)

13 A 1.8-V embedded 18-Mb DRAM macro with a 9-ns RAS access time memory cell efficiency of 33%

Yokoyama, Y.; Itoh, N.; Katayama, M.; Takashima, K.; Akasaki, H.; Kaneda, Ueda, T.; Tanaka, Y.; Yamasaki, E.; Todokoro, M.; Toriyama, K.; Miki, H.; Yamada, M.; Kobayashi, T.; Miyaoka, S.; Tamba, N.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Pages:279 - 282

[\[Abstract\]](#) [\[PDF Full-Text \(416 KB\)\]](#) [IEEE CNF](#)

14 On-line partial discharge measurement of turbine generators with noise rejection techniques on pulse-by-pulse basis

Itoh, R.; Kaneda, Y.; Kitamura, S.; Kimura, K.; Otoba, K.; Tanaka, T.; Tokura, Okada, I.;
Electrical Insulation, 1996., Conference Record of the 1996 IEEE International Symposium on , Volume: 1 , 16-19 June 1996
Pages:197 - 200 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(320 KB\)\]](#) [IEEE CNF](#)

15 Distributed shared memory architecture for JUMP-1 a general-purpose MPP prototype

Matsumoto, T.; Kudoh, T.; Nishimura, E.; Hiraki, K.; Amano, H.; Tanaka, H.;
Parallel Architectures, Algorithms, and Networks, 1996. Proceedings. Second

International Symposium on , 12-14 June 1996
Pages:131 - 137

[\[Abstract\]](#) [\[PDF Full-Text \(644 KB\)\]](#) [IEEE CNF](#)

[1](#) [2](#) [3](#) [Next](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) |
[New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved